ATTORNEY DOCKET NO.
AUS920030722US1 (IBM2811000)

PATENT APPLICATION
SERIAL NO. 10/733,839

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of: Sang Hoo Dong et al.	§	Confirmation No.: **2202**
	§	
Serial Number: 10/733,839	§	
	§	Group Art Unit: 2193
Filed: December 11, 2003	§	
	§	
For: HIGH SPEED ADDER DESIGN FOR A MULTIPLY-ADD BASED FLOATING POINT UNIT	§	Examiner: Tan V. MAI
	§	

Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, Virginia 22313-1450

CERTIFICATE OF EFS-WEB TRANSMISSION

Pursuant to 37 C.F.R. § 1.8, I hereby certify that this correspondence is being electronically transmitted to the United States Patent and Trademark Office at www.uspto.gov

on: December 18, 2007

/Bradley D. Ellis/
Bradley D. Ellis

APPLICANTS' APPEAL BRIEF

Applicant-inventors ("Applicants") and assignee International Business Machines Corporation respectfully submit the present brief in support of the patentability of the claims of the above-referenced application.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, of Armonk, New York, assignee of the interests in the invention from the named inventors.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF CLAIMS

Claims 1-8, 10, 13, 14, 16-19, 21-23, 25, 28 and 29 are pending. Of these, Claims 1 and 16 are independent Claims. Claims 9, 11, 12, 15, 20, 24, 26, 27 and 30 have been canceled. All pending Claims have been rejected under 35 U.S.C. § 101. Applicants appeal the Examiner's rejections of the Claims under 35 U.S.C. § 101.

IV. STATUS OF AMENDMENTS

The Claims stand as amended in the September 18, 2007 Response ("Second Response") to the June 19, 2007 Final Office Action ("Final Action"). All amendments to the Claims have been entered, as indicated by the September 28, 2007 Advisory Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Floating Point Units (FPUs), which perform mathematically intensive operations on the bits of a floating point numbers, have been an element of computer architecture for years. *See* Application, page 1, lines 13-16. One aspect of the calculation is the identification of a carry operation, which indicates that a number is larger than reflected in the original number of bits used to hold the number. Thus, keeping track of a carry operation is needed to ensure proper calculations of floating point numbers. *See* Application, page 4, lines 4-15.

The present invention, defined in the Claims, improves the speed of an FPU by performing certain operations simultaneously, which reduces computation time. *See* Application,

page 16, lines 9-14. *See also*, Application, page 15, lines 10-12. The Claims embody the invention as follows, shown with illustrative citations to drawing element, paragraph, page and line numbers in the Original Application, designated in curved braces ("{}"):

1. An apparatus {200} configured to compute a result of a floating-point operation, wherein the apparatus receives an aligned addend comprising a plurality of bits and a plurality of products, the apparatus comprising:

a compound incrementer {20} coupled to receive at least some of the plurality of bits of the aligned addend and a control signal {page 13, lines 5-10}, and configured to produce an output dependent upon the received bits of the aligned addend and the control signal {page 15, lines 1-4};

a compression counter {25} coupled to receive at least some of the plurality of bits of the aligned addend and the products and configured to produce an output dependent upon the received bits of the aligned addend and the received products {page 14, lines 11-15};

a compound adder {26} coupled to receive the output of the compression counter and configured to produce an output dependent upon the output of the compression counter {page 14, lines 15-19};

a carry network {27} coupled to receive sign bits of the products and the output of the compression counter and configured to produce an output signal and a carry signal dependent upon the received sign bits of the products and the received output of the compression counter {page 15, lines 10-14};

a selector {24} coupled to receive at least some of the plurality of bits of the aligned addend and the output signal and the carry signal produced by the carry network, wherein the selector is configured to produce a selection signal dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal {page 15, line 20 to page 16, line 9}; and

a plurality of multiplexers (muxes) {22 and 23} coupled to receive the output of the compound incrementer, the output of the compound adder, and the selection signal produced by the selector, and configured to produce the result by selecting between the received output of the compound incrementer and the received output of the compound adder dependent upon the selection signal produced by the selector {page 16, line 16 to page 17, line 5}.

16. A computer program product, embodied on a computer readable medium, for computing a result of a floating-point operation, wherein the computer program product receives an aligned addend comprising a plurality of bits and a plurality of products, the computer program comprising:

computer readable program code means for operating as a compound incrementer, wherein the compound incrementer receives at least some of the plurality of bits of the aligned addend and a control signal, and produces an output dependent upon the received bits of the aligned addend and the control signal {page 13, lines 5-10 and page 15, lines 1-4};

computer readable program code means for operating as a compression counter, wherein the compression counter receives at least some of the plurality of bits of the aligned addend and the products and produces an output dependent upon the received bits of the aligned addend and the received products {page 14, lines 11-15};

computer readable program code means for operating as a compound adder that receives the output of the compression counter and produces an output dependent upon the output of the compression counter {page 14, lines 15-19};

computer readable program code means for operating as a carry network, wherein the carry network receives sign bits of the products and the output of the compression counter and produces an output signal and a carry signal dependent upon the received sign bits of the products and the received output of the compression counter {page 15, lines 10-14};

computer readable program code means for operating as a selector, wherein the selector receives at least some of the plurality of bits of the aligned addend and the output signal and the carry signal produced by the carry network, and wherein the selector produces a selection signal dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal {page 15, line 20 to page 16, line 9}; and

computer readable program code means for operating as a plurality of multiplexers (muxes), wherein the plurality of muxes receive the output of the compound incrementer, the output of the compound adder, and the selection signal produced by the selector, and produce the result by selecting between the received output of the compound incrementer and the received output of the compound adder dependent upon the selection signal produced by the selector {page 16, line 16 to page 17, line 5}.

VI. GROUNDS OF REJECTION TO BE REVIEWED

A. Whether Claims 1-8, 10, 13, 14, 16-19, 21-23, 25, 28 and 29 stand properly rejected under 35 U.S.C. § 101.

VII. ARGUMENT

A. Grouping of Claims

Claims 1 and 16 are independent. For purposes of this appeal, Applicants consider each of the independent Claims, and their respective dependent Claims, as separate groups. Thus, the groups of Claims are (A) 1-8, 10, 13 and 14; and (B) 16-19, 21-23, 25, 28 and 29.

B. Summary of Pertinent Prosecution

Applicants filed the present application on December 11, 2005, with 30 claims.

The Examiner mailed the First Action on January 3, 2007, rejecting all Claims 1-18 under 35 U.S.C. §§ 101 and 112.

Applicants responded with the First Response on April 3, 2007, amending Claims 1-4, 5-8, 10, 16-19, 21-23, 25, 28 and 29, canceling Claims 9, 11, 12, 15, 20, 24, 26, 27 and 30, and further arguing the 35 U.S.C. §§ 101 and 112 rejections.

The Examiner mailed the Final Action under appeal on June 19, 2007, finally rejecting Claims 1-8, 10, 13, 14, 16-19, 21-23, 25, 28 and 29 under 35 U.S.C. § 101.

On June 27, 2007, Applicants' representative and the Examiner held a telephone interview to discuss the rejections, and on September 18, 2007, Applicants filed their Second Response, amending Claims 1 and 16, and further arguing the 35 U.S.C. § 101 rejections.

The Examiner mailed an Advisory Action on September 28, 2007, maintaining the 35 U.S.C. § 101 rejections. This appeal followed.

C. The Examiner's Rejections Were Procedurally and Factually in Error

1. The Form and Content of the Examiner's Rejections under 35 U.S.C. § 101 Were Improper and Insufficient

a. Legal Requirements for a 35 U.S.C. § 101 Rejection

According to M.P.E.P. § 2106.IV.B, the burden is on the USPTO to set forth a *prima facie* case of unpatentability. Therefore if USPTO personnel determine that it is more likely than not that the claimed subject matter falls outside all of the statutory categories, they must provide an explanation. Any rejection based on lack of utility should include a detailed explanation why the claimed invention has no specific and substantial credible utility. M.P.E.P. § 2107.II(C) Further, for claims rejected under 35 U.S.C. § 101, USPTO personnel are to identify the features

of the invention that would render the claimed subject matter statutory if recited in the claim. M.P.E.P. § 2106.IV.B.

For an invention to be "useful" it must satisfy the utility requirement of § 101. The USPTO's official interpretation of the utility requirement provides that the utility of an invention has to be (i) specific, (ii) substantial and (iii) credible. M.P.E.P. § 2106.IV.C.2(2)(a), citing *In re Fisher*, 421 F.3d 1365 at 1372 (Fed. Cir. 2005). "The plain and unambiguous meaning of § 101 is that any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may be patented if it meets the requirements for patentability set forth in Title 35 …." *In re Alappat*, 33 F.3d 1526 at 1542 (Fed. Cir. 1994) (*en banc*). As the Supreme Court has recognized, Congress chose the expansive language of 35 U.S.C. § 101 so as to include "anything under the sun that is made by man" as statutory subject matter. *Diamond v. Chakrabarty*, 447 U.S. 303 at 308-09 (1980).

To properly determine whether a claimed invention complies with the statutory invention requirements of 35 U.S.C. § 101, USPTO personnel must first identify whether the claim falls within at least one of the four enumerated categories of patentable subject matter recited in section 101 (i.e., process, machine, manufacture, or composition of matter). M.P.E.P. § 2106.IV.B. Thus, in order to support a rejection under 35 U.S.C. § 101, the Examiner is obliged to a set forth a *prima facie* case of unpatentability, showing that it is more likely than not that the claimed subject matter falls outside all of the statutory categories, and provide an explanation.

b. The Examiner's Stated Grounds Were Insufficient

As described above, the Examiner has rejected all pending Claims under 35 U.S.C. § 101. Specifically, the Examiner alleges a lack of a useful result. Final Action, page 3. The Examiner

concedes that the claims "appear to be concrete and tangible." *Id.* The Examiner addresses only independent Claims 1 and 16, dependent Claims 2-8, 10, 13, 14, 17-19, 21-23, 25, 28 and 29 are rejected because of their dependence from one of Claims 1 and 16.

Independent Claim 1 recites "An *apparatus* configured to compute *a result of a floating-point operation* ... comprising ... a plurality of multiplexers ... configured to produce *the result* by selecting between the received output of the compound incrementer and the received output of the compound adder ...." (emphasis added) Applicant respectfully asserts that, by reciting an *apparatus*, Claim 1 falls within at least two enumerated statutory categories: machine and manufacture. Further, Claim 1 clearly recites that the apparatus produces a result: the computed result of a floating point operation. Applicant also respectfully asserts that an apparatus that is configured to compute a floating point operation produces a useful result.

Applicant asserts that floating point units (FPUs) are common, well known elements of computer architecture, and are also well known in the art as providing a useful result. Applicant notes that the Examiner has not provided a detailed explanation as to why an apparatus configured to provide an improved computation of a floating point operation, is not useful, as required by the M.P.E.P. Further, the Examiner has also failed to identify any further features that the Examiner would deem as rendering the claimed subject matter statutory, as required by the M.P.E.P.

In view of the foregoing, it is apparent that the 35 U.S.C. § 101 rejection of Claim 1 is improper. Dependent Claims 2-8, 10, 13, and 14 depend from Claim 1, and are thus patentable for, at least, their dependence from a patentable base claim.

Independent Claim 16 recites "A computer program product, embodied on a computer readable medium, for computing a result of a floating-point operation ... comprising ...

computer readable program code means for operating as a plurality of multiplexers (muxes), wherein the plurality of muxes ... produce the result ...." As with Claim 1 above, the Examiner alleges that Claim 16 does not recite a practical application that produces a useful result. The Examiner further asserts that the "applicant might have meant to include transmission media and signals, since program can be embodied on waves." Final Action, page 3.

Applicant respectfully asserts that providing for an improved floating point computation is a useful result, and that since Claim 16 recites a computer program product embodied on a computer readable medium, Claim 16 falls within at least the enumerated statutory category of machine. Applicant notes that Claim 16 recites that "wherein the computer program product receives an aligned addend comprising a plurality of bits and a plurality of products" and thus it is clear that Applicant has not attempted to claim transmitted signals or waves.

In view of the foregoing, it is apparent that the 35 U.S.C. § 101 rejection of Claim 16 is improper. Dependent Claims 17-19, 21-23, 25, 28 and 29 depend from Claim 16, and are thus patentable for, at least, their dependence from a patentable base claim.

Applicants respectfully submit that the Examiner's stated grounds are insufficient to maintain the 35 U.S.C. § 101 rejections of Claims 1-8, 10, 13, 14, 16-19, 21-23, 25, 28 and 29. Therefore, Applicants respectfully request that the 35 U.S.C. § 101 rejections of Claims 1-8, 10, 13, 14, 16-19, 21-23, 25, 28 and 29 be reversed.

VIII. CLAIMS APPENDIX

See Attached.

IX. EVIDENCE APPENDIX

NONE.

X. RELATED PROCCEDINGS APPENDIX

NONE.

XI. CONCLUSION

For the foregoing reasons, it is respectfully submitted that the Final Rejections of Claims 1-8, 10, 13, 14, 16-19, 21-23, 25, 28 and 29 under 35 U.S.C. § 101 are improper and should be reversed. Applicants respectfully request that the rejections of Claims 1-8, 10, 13, 14, 16-19, 21-23, 25, 28 and 29 be withdrawn and that these Claims be allowed.

Respectfully submitted,

CARR LLP

Dated: December 18, 2007
CARR LLP
670 Founders Square
900 Jackson Street
Dallas, Texas 75202
Telephone: (214) 760-3030
Fax: (214) 760-3003

/Gregory W. Carr/
Gregory W. Carr
Reg. No. 31,093

VIII – APPENDIX – CLAIMS ON APPEAL

1. (Previously Presented) An apparatus configured to compute a result of a floating-point operation, wherein the apparatus receives an aligned addend comprising a plurality of bits and a plurality of products, the apparatus comprising:

a compound incrementer coupled to receive at least some of the plurality of bits of the aligned addend and a control signal, and configured to produce an output dependent upon the received bits of the aligned addend and the control signal;

a compression counter coupled to receive at least some of the plurality of bits of the aligned addend and the products and configured to produce an output dependent upon the received bits of the aligned addend and the received products;

a compound adder coupled to receive the output of the compression counter and configured to produce an output dependent upon the output of the compression counter;

a carry network coupled to receive sign bits of the products and the output of the compression counter and configured to produce an output signal and a carry signal dependent upon the received sign bits of the products and the received output of the compression counter;

a selector coupled to receive at least some of the plurality of bits of the aligned addend and the output signal and the carry signal produced by the carry network, wherein the selector is configured to produce a selection signal dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal; and

a plurality of multiplexers (muxes) coupled to receive the output of the compound incrementer, the output of the compound adder, and the selection signal produced by the selector, and configured to produce the result by selecting between the received output of the compound incrementer and the received output of the compound adder dependent upon the selection signal produced by the selector.

2. (Previously Presented) The apparatus of Claim 1, wherein the compound incrementer further comprises:

an incrementer coupled to receive at least some of the plurality of bits of the aligned addend and configured to produce an output dependent upon the received bits of the aligned addend and the control signal; and

a plurality of negation devices.

3. (Previously Presented) The apparatus of Claim 2, wherein one of the negation devices is coupled to receive the output of the incrementer and the control signal, and is configured to produce an output dependent upon the received output of the incrementer and the control signal.

4. (Previously Presented) The apparatus of Claim 2, wherein the plurality of negation devices implement exclusive-OR (XOR) logic functions.

5. (Original) The apparatus of Claim 2, wherein the plurality of negation devices are XOR-gates.

6. (Previously Presented) The apparatus of Claim 1, wherein the carry network further comprises:

logic coupled to receive the sign bits of the products and configured to produce the output signal dependent upon the received sign bits of the products; and

a carry generator coupled to receive the output of the compression counter and configured to produce the carry signal dependent upon the received output of the compression counter.

7. (Previously Presented) The apparatus of Claim 1, wherein the carry network further comprises:

an XOR-gate coupled to receive the sign bits of the products and configured to produce the output signal dependent upon the received sign bits of the products; and

a carry generator coupled to receive the output of the compression counter and configured to produce the carry signal dependent upon the received output of the compression counter.

8. (Previously Presented) The apparatus of Claim 1, wherein the selector is configured to produce a plurality of selection signals dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal.

9. (Canceled).

10. (Previously Presented) The apparatus of Claim 1, wherein the output of the compound adder comprises a sum signal and an incremented sum signal, and one of the plurality of muxes is coupled to receive the sum signal from the compound adder, the incremented sum signal from the compound adder, and an inverted version of the sum signal , and is configured to produce at least a portion of the result.

11. (Canceled).

12. (Canceled).

13. (Original) The apparatus of Claim 1, wherein the compression device further comprises a 3:2 Counter.

14. (Original) The apparatus of Claim 4, wherein the compression device further comprises a 3:2 Counter.

15. (Canceled).

16. (Previously Presented) A computer program product, embodied on a computer readable medium, for computing a result of a floating-point operation, wherein the computer program product receives an aligned addend comprising a plurality of bits and a plurality of products, the computer program comprising:

computer readable program code means for operating as a compound incrementer, wherein the compound incrementer receives at least some of the plurality of bits of the aligned addend and a control signal, and produces an output dependent upon the received bits of the aligned addend and the control signal;

computer readable program code means for operating as a compression counter, wherein the compression counter receives at least some of the plurality of bits of the aligned addend and the products and produces an output dependent upon the received bits of the aligned addend and the received products;

computer readable program code means for operating as a compound adder that receives the output of the compression counter and produces an output dependent upon the output of the compression counter;

computer readable program code means for operating as a carry network, wherein the carry network receives sign bits of the products and the output of the compression counter and produces an output signal and a carry signal dependent upon the received sign bits of the products and the received output of the compression counter;

computer readable program code means for operating as a selector, wherein the selector receives at least some of the plurality of bits of the aligned addend and the output signal and the carry signal produced by the carry network, and wherein the selector produces a selection signal dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal; and

computer readable program code means for operating as a plurality of multiplexers (muxes), wherein the plurality of muxes receive the output of the compound incrementer, the output of the compound adder, and the selection signal produced by the selector, and produce the result by selecting between the received output of the compound incrementer and the received output of the compound adder dependent upon the selection signal produced by the selector.

17. (Previously Presented) The computer program product of Claim 16, wherein the computer readable program code means for operating as compound incrementer further comprises:

computer readable program code means for operating as an incrementer, wherein the incrementer receives at least some of the plurality of bits of the aligned addend and produce an output dependent upon the received bits of the aligned addend and the control signal; and

computer readable program code means for operating as a plurality of negation devices.

18. (Previously Presented) The computer program product of Claim 17, wherein one of the negation devices receives the output of the incrementer and the control signal, and produces an output dependent upon the received output of the incrementer and the control signal.

19. (Previously Presented) The computer program product of Claim 17, wherein the computer readable program code means for operating as the plurality of negation devices comprises computer readable program code means for implementing exclusive-OR (XOR) logic functions.

20. (Canceled).

21. (Previously Presented) The computer program product of Claim 16, wherein the computer readable program code means for operating as the carry network further comprises:

computer readable program code means for operating as logic receiving the sign bits of the products and producing the output signal dependent upon the received sign bits of the products; and

computer readable program code means for operating as a carry generator, wherein the carry generator receives the output of the compression counter and produces the carry signal dependent upon the received output of the compression counter.

22. (Previously Presented) The computer program product of Claim 16, wherein the computer readable program code means for operating as carry network further comprises:

computer readable program code means for operating as an XOR-gate, wherein the XOR-gate receives the sign bits of the products and produces the output signal dependent upon the received sign bits of the products; and

a computer readable program code means for operating as a carry generator, wherein the carry generator receives the output of the compression counter and produces the carry signal dependent upon the received output of the compression counter.

23. (Previously Presented) The computer program product of Claim 16, wherein the selector produces a plurality of selection signals dependent upon the received bits of the aligned addend, the received output signal, and the received carry signal.

24. (Canceled).

25. (Previously Presented) The computer program product of Claim 16, wherein the output of the compound adder comprises a sum signal and an incremented sum signal, and one of the plurality of muxes is coupled to receive the sum signal from the compound adder, the incremented sum signal from the compound adder, and an inverted version of the sum signal, and is configured to produce at least a portion of the result.

26. (Canceled).

27. (Canceled).

28. (Previously Presented) The computer program product of Claim 16, wherein the computer readable program code means for operating as compression device further comprises computer readable program code means for operating as 3:2 Counter.

29. (Previously Presented) The computer program product of Claim 19, wherein the computer readable program code means for operating as compression device further comprises computer readable program code means for operating as 3:2 Counter.

30. (Canceled).